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CATEGORY:

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PATENT APPLICATION

ATTORNEY DOCKET NO. 10961260-1

12/21/98 U.S. PTO

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

JC525 U.S. PTO 09/217740 12/21/98

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Min Cao et al**

TITLE: **Local Oxidation Of A Sidewall Sealed Shallow Trench For Providing Isolation Between Devices Of A Substrate**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 5 sheets of drawings (one set)

( ) Information Disclosure Statement and Form PTO-1449 ( ) Associate Power of Attorney

( ) Priority document(s) ( ) (Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	9 — 20	0	X $ 18	$ 0
INDEPENDENT CLAIMS	3 — 3	0	X $ 78	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$ 260	$ 0
BASIC FEE: Design ($310.00); Utility ($760.00)				$ 760
TOTAL FILING FEE				$ 760
OTHER FEES				$
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 760

Charge $ 760 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17,1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EM 155 891 295 US

Date of Deposit December 21, 1998

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By Nelia T. de Guzman

Typed Name: **Nelia T. de Guzman**

Respectfully submitted,

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By Brian R. Short

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Rev 11/98 (TransNew)

- Attach as First Page to Transmitted Papers -

LOCAL OXIDATION OF A SIDEWALL SEALED SHALLOW TRENCH FOR PROVIDING ISOLATION BETWEEN DEVICES OF A SUBSTRATE

FIELD OF INVENTION

This invention relates generally to semiconductor device isolation. In particular, it relates to local oxidation of a sidewall sealed shallow trench for providing isolation between devices formed in a substrate.

BACKGROUND

Integrated circuits include substrates which generally include active devices formed in proximity to each other. Increasing the density of active devices included on a substrate requires the active devices to be formed more closely to each other. If the active devices are too close to each other, the active devices can electrically connect to each other. Alternatively, signals from one active device can couple to a neighboring active device. This coupling or crosstalk can degrade the performance of the active devices. Therefore, typically some type of isolation structure must be formed between active devices to prevent the active devices from being electrically connected and to prevent coupling of signals between the active devices.

Figure 1 shows a first type of isolation structure 8 typically used to isolate active devices of a substrate 10. The isolation structure 8 shown in Figure 1 is formed using a local oxidation of silicon (LOCOS) technique. LOCOS isolation structures include the surface of an active semiconductor substrate 10 being oxidized between active device regions 12, 14 of the semiconductor substrate 10 surface to help prevent electronic interactions between adjacent active device regions 12, 14.

The effectiveness of LOCOS isolation structures degrades significantly as the active device regions 12, 14 become closer together due to parasitic currents that can develop between adjacent devices 12, 14 beneath the LOCOS structures. Additionally, the LOCOS isolation structure 8 is too wide to allow the active device regions 12, 14 to be formed too close to each other.

Figure 2 shows a second type of isolation structure typically used to isolate active device regions 24, 26 of a substrate 20. The isolation structure shown in Figure 2 is formed by etching a trench 22 in a silicon substrate 20 between the active device regions 24, 26, and filling the trench 22 with an isolation material such as silicon oxide. Generally, the deeper the trench 22, the greater the isolation between the active device regions 24, 26. Generally, the narrower the trench 22, the closer the active device regions 24, 26 can be with respect to each other. However, if the trench 22 is deep and narrow, the trench 22 can be very difficult to form. That is, deep narrow trenches can be difficult to properly fill with an isolation material.

It is desirable to have a substrate isolation structure which allows active device regions of the substrate to be formed close to each other while still maintaining isolation between the active device regions. It is desirable that the substrate isolation structure provide more isolation between the active device regions than LOCOS isolation and trench isolation structures.

SUMMARY OF THE INVENTION

The present invention is an substrate isolation method and structure which allows active device regions of the substrate to be formed close to each other while still maintaining isolation between the active device regions. The substrate isolation structure provides more isolation between the active device regions than LOCOS isolation and trench isolation structures.

A first embodiment of this invention includes semiconductor isolation structure. The semiconductor isolation structure includes a substrate. A first device and a second device are formed within the substrate. An isolation region is formed within the substrate between the first device and the second device. The isolation region includes a deep region which extends into the substrate. The deep region includes a deep region cross-sectional area. A shallow region extends to the surface of the substrate. The shallow region includes a shallow region cross-sectional area. The deep region cross-sectional area is greater than the shallow region cross-sectional area.

A second embodiment includes a semiconductor isolation structure. The semiconductor isolation structure includes a substrate. A first device and a second device are formed within the

substrate. An isolation region is formed within the substrate between the first device and the second device. The isolation region includes an deep region which extends into the substrate. The deep region includes an oxide. A shallow region extends to the surface of the substrate. The shallow region includes a protective wall. The protective wall can be formed from an oxide and a nitride.

A third embodiment includes method of forming an isolation structure within a substrate. The method includes forming a trench in the substrate. A protective wall layer is formed within the trench. A bottom portion of the protective wall layer is removed exposing a surface of the substrate. The exposed surface of the substrate is directly oxidized. Finally, the trench is filled with an isolation material. The isolation material can be an oxide.

A fourth embodiment is similar to the third embodiment. The the step of removing a bottom portion of the protective wall layer exposing a surface of the substrate of the fourth embodiment includes removing the bottom portion of the protective wall layer exposing the substrate, and forming a second trench in the exposed substrate forming an exposed surface.

Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art LOCOS isolation structure.

Figure 2 shows a prior art trench isolation structure

Figure 3 shows an embodiment of the invention.

Figure 4 shows a substrate in which an oxide layer and a nitride layer have been deposited.

Figure 5 shows a first trench having been etched through the oxide layer, the nitride layer and into the substrate.

Figure 6 shows an oxide layer grown on a substrate surface exposed during the formation of the first trench.

Figure 7 shows the nitride layer and the oxide layer having been etched at the bottom of the first trench.

Figure 8 shows the exposed substrate at the bottom of the first trench having been directly oxidized.

Figure 9 shows the first trench having been filled with an oxide and then polished down to the surface of the substrate.

Figure 10 shows the trench formed by the processing step of Figure 7, in which a second trench is etched further into the exposed substrate at the bottom of the first trench.

Figure 11 shows the exposed substrate at the bottom of the second trench having been directly oxidized.

Figure 12 the first trench and the second trench having been filled with an oxide and then polished down to the surface of the substrate 300.

DETAILED DESCRIPTION

As shown in the drawings for purposes of illustration, the invention is embodied in a method and structure for isolating active device regions of a substrate. The isolation structure of the invention provides for an isolation structure which is deeper than LOCOS or trench isolation structures. The isolation structure includes a unique shape which increase the isolation provided by the isolation structure.

Figure 3 shows an embodiment of the invention. This embodiment includes a isolation region formed in a substrate 300. The isolation region includes an deep region 308 and a

shallow region 306. Generally, the isolation region is formed between active device regions 302, 304 of the substrate 300.

The shallow region 306 extends to the surface of the substrate 300. The shallow region 306 includes a wall which generally includes a first wall material 320 and a second wall material 330. The existence of the wall is a result of the unique processing steps used to form the isolation region. The unique processing steps provide the unique structure of the isolation region according to the invention. The presence of the wall allow for formation of a deeper isolation region than prior art LOCOS and prior art trench isolation structures.

Generally, the first wall material 320 consists of a silicon nitride material. Generally, the second wall material 330 consists of an oxide material. Other types of materials can be used for the first wall material 320 and the second wall material 330.

The first wall material 320 provides a sealing function which is utilized during the fabrication of the isolation region to allow for the fabrication of the deep region 308. Fabrication of the deep region 308 will be discussed later.

The second wall material 330 provides stress relief between the silicon nitride first wall 320 and the substrate 300. The second wall material 330 also provides a low defect density between the second wall and the substrate 300. Without the second wall material 330, the silicon nitride first wall 320 would directly contact the substrate 300, which is undesirable.

The formation of the deep region 308 provides for a deeper isolation structure than presently existing isolation structures. In addition, the deep region 308 includes a deep region cross-sectional area 335 which can be larger than a shallow region cross-sectional area 337 of the shallow region 306. The deep region cross-sectional area 335 of the deep region 308 being larger than the shallow region cross-sectional area 337 of the shallow region 304 improves the isolation between the active device regions 302, 304.

A dashed line 340 of Figure 3 shows the path of leakage current between a p-doped active device region 304 and a P-type substrate 300. Without the unique wide deep region cross-sectional area 335 of the deep region 308 of the invention, the length of the dashed line 340 representing the path of the leakage current would be much shorter. The result being reduced isolation between the active device regions 302, 304.

The embodiment shown in Figure 3 includes a P-type substrate, an N-well, a P-well, a p-doped active device region 304 and an n-doped active device region 304. This configuration is shown merely as an example of the type of active device regions the isolation structure according to the invention can be used to isolate. The isolation structure of the invention can be used to isolate other types of active device regions as well.

Figures 4-9 show processing steps which may be used to form the embodiment shown in Figure 3.

Figure 4 shows a substrate 300 in which a silicon oxide layer 410 has been thermally grown and a silicon nitride layer 420 has been deposited. Thermally growing silicon oxide is well known in the art of semiconductor processing. The silicon nitride layer is deposited through a low pressure chemical vapor deposition (LPCVD) process. LPCVD is well known in the art of semiconductor processing.

Figure 5 shows a trench 510 having been etched through the oxide layer 410, the nitride layer 420 and into the substrate 300. The shape and location of the trench are determined through photo lithography. Photo lithography generally includes the deposition and removal of a resist layer. Photo lithography is well known in the art of semiconductor processing.

Figure 6 shows an oxide layer 610 grown on a surface of the substrate 300 exposed during the formation of the trench 510. A nitride layer 620 is deposited over the oxide layer 610 and the nitride layer 420. Again, the oxide layer 610 is thermally grown. The nitride layer 620 is generally deposited using LPCVD.

Figure 7 shows the nitride layer 620 and the oxide layer 610 having been etched exposing the bottom of the trench 510. The oxide layer 610 is generally dry etched.

Figure 8 shows the exposed substrate at the bottom of the trench having been directly oxidized. Again, the direct oxidation is typically thermally grown.

Figure 9 shows the trench having been filled with an oxide 910 and then polished down to the surface of the substrate 300. The remaining portions of the nitride layer 620 and the oxide layer 610 form shallow region walls 920, 930. The oxide 910 is generally deposited by LPCVD. The oxide 910 is polished by a chemical mechanical polish (CMP) process. The shallow region wall 920 corresponds with the second wall material 330 of the embodiment shown in Figure 3. The shallow region wall 930 corresponds with the first wall material 320 of the embodiment shown in Figure 3.

Figures 10-12 show the processing steps of an alternate embodiment of the invention.

Figure 10 shows the trench formed by the processing step of Figure 7, in which a second trench 1010 is etched further into the exposed substrate at the bottom of the original trench. Again, the shape and location of the second trench 1010 are determined through photo lithography. The second trench 1010 is generally formed by a dry etch process.

Figure 11 shows the exposed substrate at the bottom of the second trench 1010 having been directly oxidized. Again, the direct oxidation is typically thermally grown.

Figure 12 both trenches 510, 1010 having been filled with an oxide 1210 and then polished down to the surface of the substrate 300. The remaining portions of the nitride layer and the oxide layer 610 form shallow region walls 1220, 1230. The oxide 1210 is generally deposited by LPCVD. The oxide 1210 is polished by a chemical mechanical polish (CMP)

process. The shallow region wall 1220 corresponds with the second wall material 330 of the embodiment shown in Figure 3. The shallow region wall 1230 corresponds with the first wall material 320 of the embodiment shown in Figure 3.

Although specific embodiments of the invention have been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.

What is claimed:

1. A semiconductor isolation structure comprising:

a substrate, the substrate comprising a surface;

a first device and a second device formed within the substrate;

an isolation region formed within the substrate between the first device and the second device, the isolation region comprising:

a deep region which extends into the substrate, the deep region comprising a deep region cross-sectional area;

a shallow region which extends to the surface of the substrate, the shallow region comprising a shallow region cross-sectional area; wherein

the deep region cross-sectional area is greater than the shallow region cross-sectional area.

2. The semiconductor isolation structure as recited in claim 1, wherein the isolation region comprises an oxide.

3. The semiconductor isolation structure as recited in claim 1, wherein the shallow region comprises a protective outer wall adjacent to the substrate.

4. The semiconductor isolation structure as recited in claim 1, wherein the protective outer wall comprises a layer of Nitride.

5. A semiconductor isolation structure comprising:

a substrate, the substrate comprising a surface;

a first device and a second device formed within the substrate;

an isolation region formed within the substrate between the first device and the second device, the isolation region comprising:

a deep region which extends into the substrate, the deep region comprising an oxide;

a shallow region which extends to the surface of the substrate, the shallow region comprising a protective wall.

6. The semiconductor isolation structure of claim 5, in which the protective wall comprises an oxide wall and a nitride wall.

7. A method of forming an isolation structure within a substrate, the method comprising:

forming a trench in the substrate;

forming a protective wall layer within the trench;

removing a bottom portion of the protective wall layer exposing a surface of the substrate;

directly oxidizing the exposed surface of the substrate;

filling the trench with oxide; and

polishing the oxide.

8. The method of forming an isolation structure within a substrate of claim 7, wherein the step of forming a protective wall within the trench comprises:

growing an oxide layer on a surface of the trench; and

depositing a nitride layer over the oxide layer.

9. The method of forming an isolation structure within a substrate of claim 7, wherein the step of removing a bottom portion of the protective wall layer exposing a surface of the substrate comprises:

removing a bottom portion of the protective wall layer exposing the substrate; and

forming a second trench in the exposed substrate forming an exposed surface.

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ABSTRACT

A semiconductor isolation structure. The semiconductor isolation structure includes a substrate. A first device and a second device are formed within the substrate. An isolation region is formed within the substrate between the first device and the second device. The isolation region includes a deep region which extends into the substrate. The deep region includes a deep region cross-sectional area. A shallow region extends to the surface of the substrate. The shallow region includes a shallow region cross-sectional area. The deep region cross-sectional area is greater than the shallow region cross-sectional area. For an alternate embodiment, the deep region includes an oxide and the shallow region includes a protective wall. The protective wall can be formed from an oxide and a nitride.

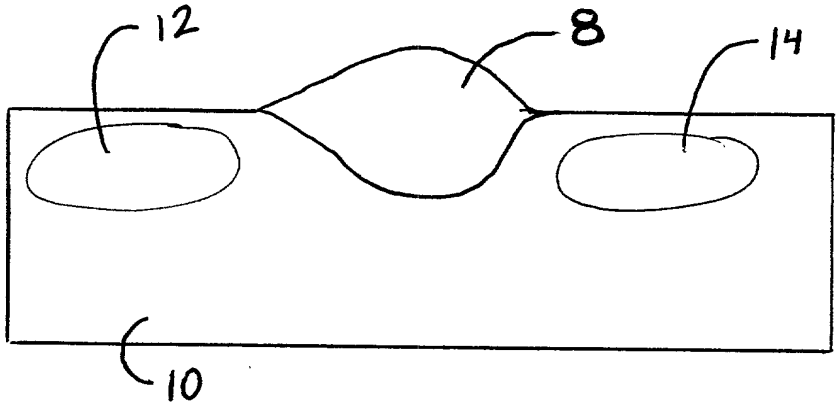

Figure 1 (Prior Art)

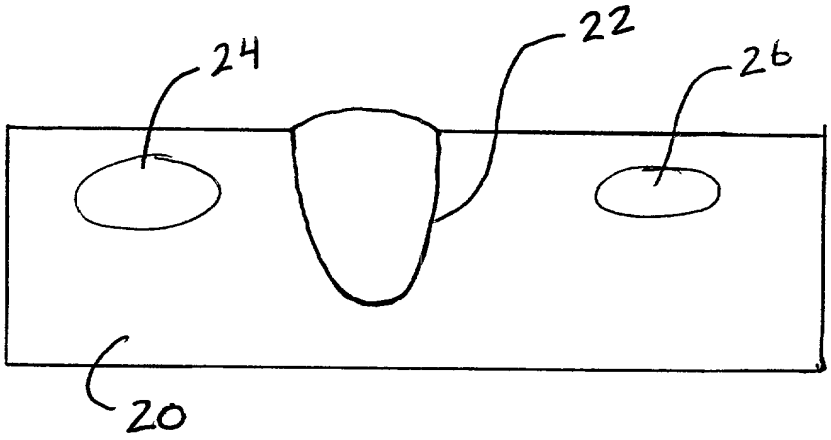

Figure 2 (Prior Art)

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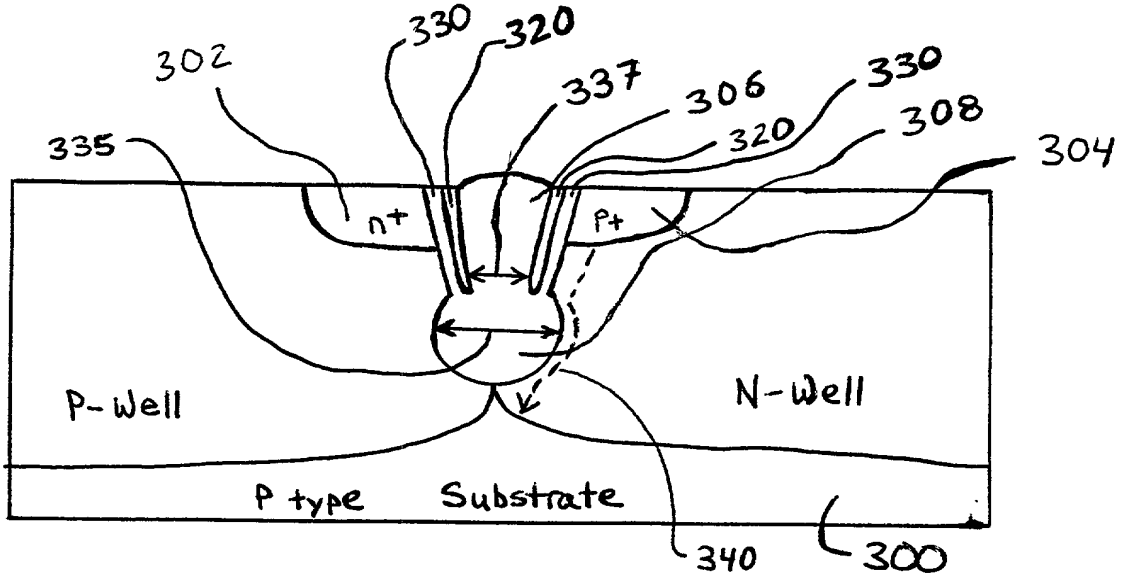

Figure 3

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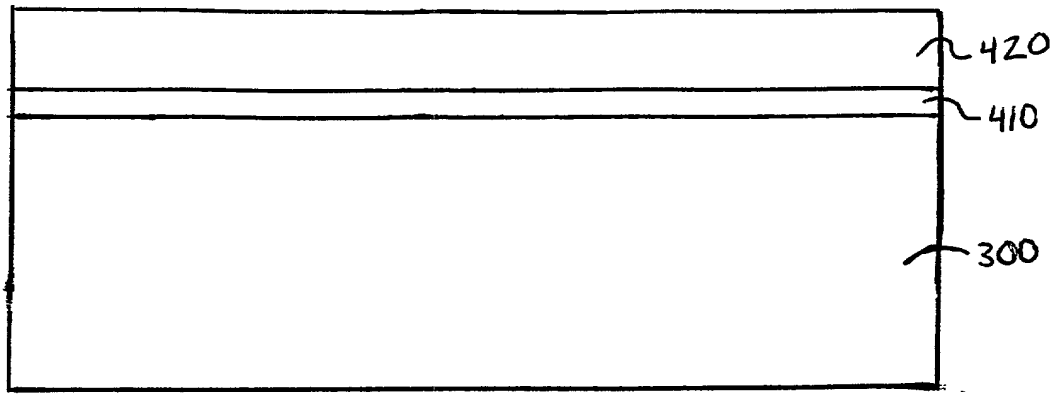

Figure 4

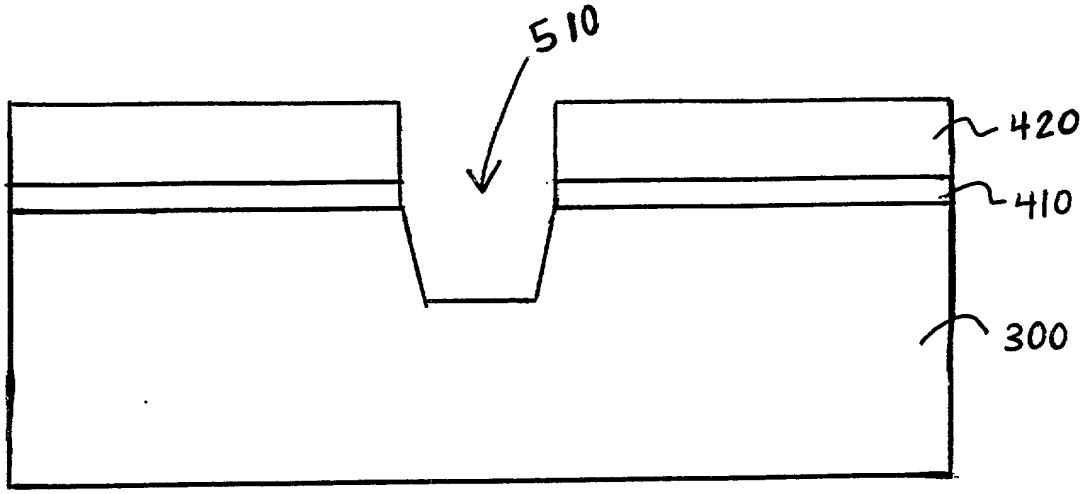

Figure 5

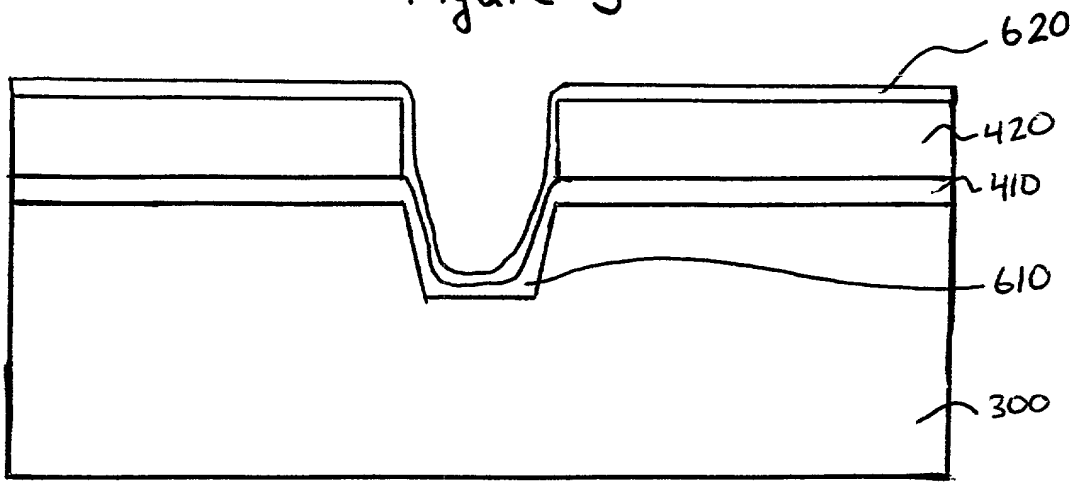

Figure 6

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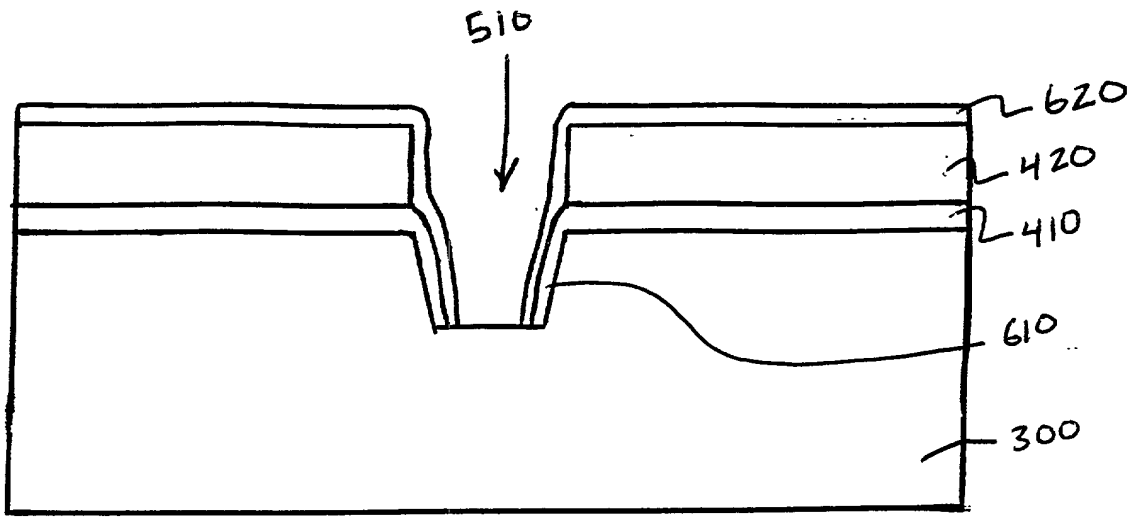

Figure 7

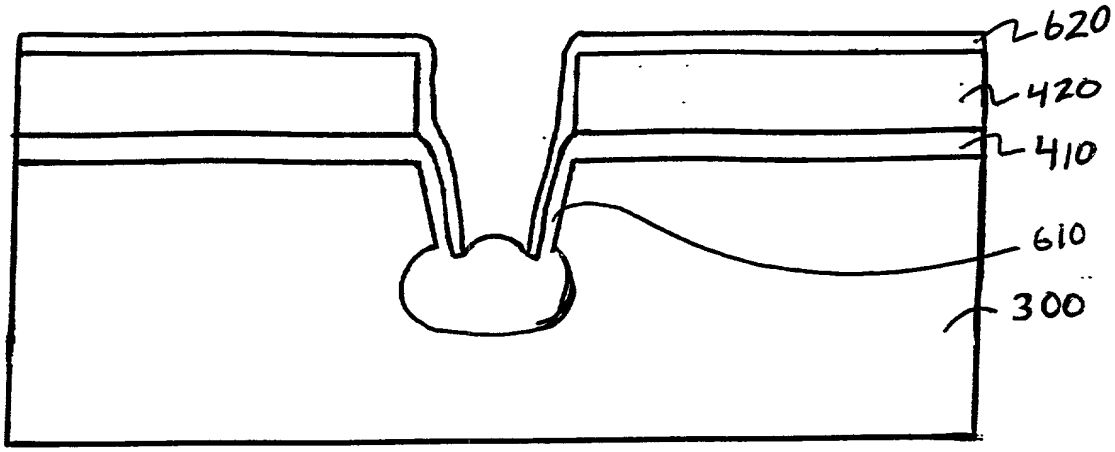

Figure 8

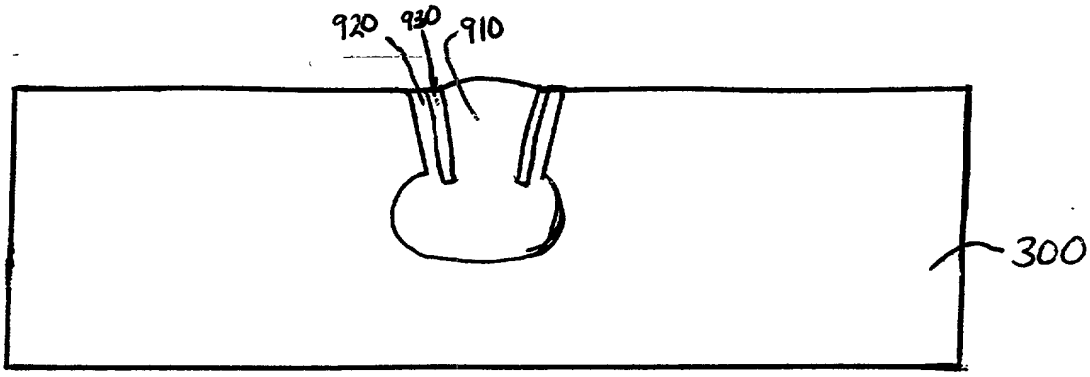

Figure 9

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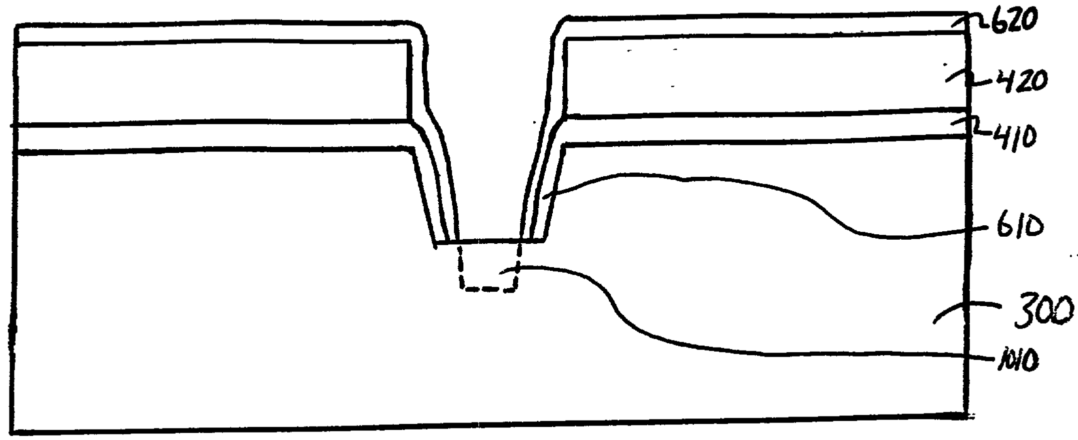

Figure 10

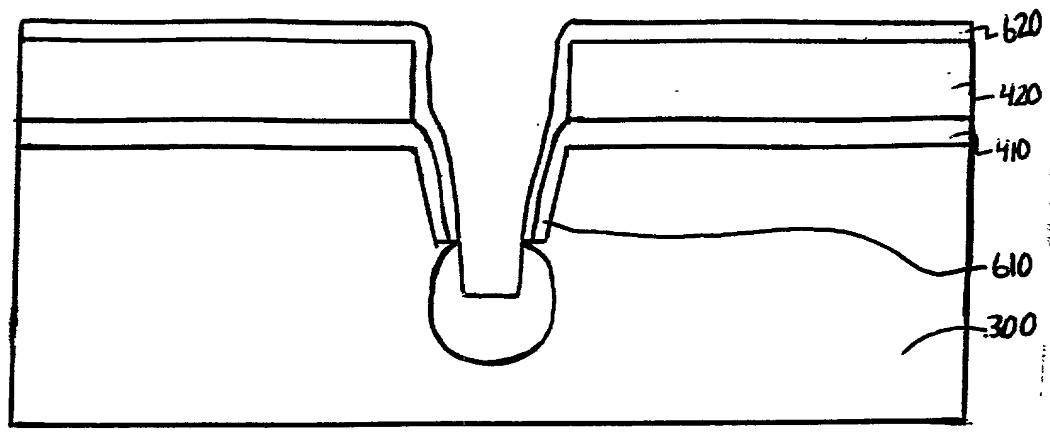

Figure 11

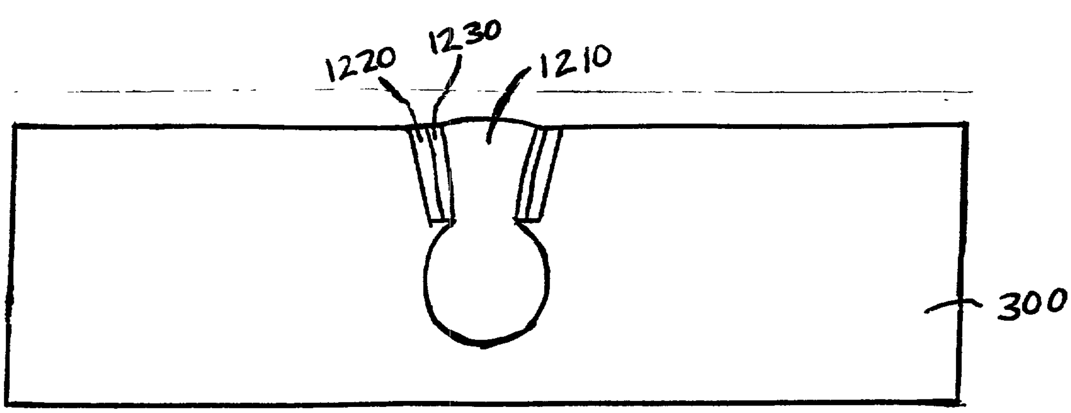

Figure 12

PATENT APPLICATION

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 10961260-1

09214740 . 122198

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Local Oxidation Of A Sidewall Sealed Shallow Trench For Providing Isolation Between Devices Of A Substrate

the specification of which is attached hereto unless the following box is checked:

( ) was filed on __________ as US Application Serial No. or PCT International Application Number __________ and was amended on __________ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Brian R. Short	**Herbert R. Schulze**	**Ian Hardcastle**	**Timothy Rex Croll**
Reg. No. **41,309**	Reg. No. **30,682**	Reg. No. **34,075**	Reg. No. **36,771**

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Min Cao — **Inventor's Signature**

12/17/98 — **Date**

Rev 11/98 (DecPwr)

(Use Page Two For Additional Inventor(s) Signature(s))

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 10961260-1

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12/17/98
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12/16/98
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Inventor's Signature

12/17/98.
Date

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Residence: _____

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Inventor's Signature

Date

Full Name of # 6 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature

Date

Full Name of # 7 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature

Date

Full Name of # 8 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature

Date